What is claimed is:

1. An interleaver for rearranging sequences of data block in a data processing system, the interleaver comprising:

a preprocessor for preparing seed variables that varies according to the interleaving method of each standard and bit rate; and

an address generator means for generating an interleaved address on the fly using the seed variables.

2. The interleaver of claim 1, wherein the number of seed variables is less than the size of block data.

3. The interleaver of claim 1, wherein the seed variables include a base column vector, an increment column vector, a cumulative column vector, and a modulo base, the number of elements of all three column vectors is equal to the number of rows of the interleaver, and the elements of the column vectors are inter-row permutated in advance at the preprocessing, and

wherein the cumulative column vector is updated by adding the increment vector to an old cumulative vector, after the interleaved addresses for one column are generated by adding the base vector and a vector that is calculated from the cumulative vector, and

wherein if elements of the updated cumulative column vector are larger than the modulo base, the elements of the updated cumulative column vector is subtracted by the modulo base.

4. A turbo decoding system comprising:

a block interleaver;

an address queue for storing the generated interleaved address equal or smaller than the size of block data;

an SISO decoder performing recursive decoding and calculating log likelihood ratio; and

an LLR memory connected to the SISO decoder and storing the log likelihood ratio,

wherein the block interleaver comprises a preprocessor for preparing seed variables and an address generator for generating an interleaved address on the fly using the seed variables,

wherein the SISO decoder accessing the data block and the log likelihood ratio in a sequential order and in an interleaved order alternately by the generated interleaved address.

5. The turbo decoding system of claim 4, wherein the generated interleaved address is once stored in the address queue and reused as a write address for writing the log likelihood ratio outputted from the SISO decoder into the LLR memory.

6. The turbo decoding system of claim 4, wherein the length of the address queue is equal to the SISO latency.

7. The turbo decoding system of claim 4, wherein the seed variables include a base column vector, an increment column vector, a cumulative column vector, and a modulo base, the number of elements of all three column vectors is equal to the number of rows of the block interleaver, and the elements of the column vectors are inter-row permutated, and

wherein the cumulative column vector is updated by adding the increment vector to the old cumulative vector, after the interleaved addresses for one column are generated by adding the base vector and a vector that is calculated from the cumulative vector, and

wherein if elements of the updated cumulative column vector are larger than the modulo base, the elements of the updated cumulative column vector is subtracted by the modulo base.

8. A turbo decoding system comprising:

a processor for generating interleaved addresses;

an address queue for storing the interleaved addresses;

a buffer memory block including an LLR memory for storing log likelihood ratio and a plurality of memory blocks for storing soft inputs; and

an SISO decoder connected to the buffer memory block, the SISO decoder including ACSA network for calculating the log likelihood ratio recursively from soft inputs and the log likelihood provided by the LLR memory and a plurality of memory blocks connected to the ACSA network.

9. The turbo decoding system of claim 8, wherein the processor prepares seed variables when an interleaver structure changes due to the change of the coding standard or bit rate, and generates the interleaved addresses column by column using the seed variables when the interleaved addresses are required.

10. The interleaving method of claim 9, wherein the seed variables include a base column vector, an increment column vector, a cumulative column vector, and a modulo base, the number of elements of all three column vectors is equal to the number of rows of the interleaver, and the elements of the column vectors are inter-row permutated, and

wherein the cumulative column vector is updated by adding the increment vector to the old cumulative vector, after the interleaved addresses for one column are generated by adding the base vector and a vector that is calculated from the cumulative vector, and

wherein if elements of the updated cumulative column vector are larger than the modulo base, the elements of the updated cumulative column vector is subtracted by the modulo base.

11. The turbo decoding system of claim 8, wherein the SISO decoder supports Viterbi decoding mode,

wherein in Viterbi decoding mode, the ACSA network performs Viterbi recursion, the LLR memory stores traceback information outputted by the ACSA network, the processor processes traceback from the traceback information read from the LLR memory, and one of the memory blocks of the SISO decoder stores path metric outputted by the ACSA network.

12. The turbo decoding system of claim 10, wherein the processor uses STOLT, SUBGE, LOOP instructions for fast calculation of interleaved addresses.

13. The turbo decoding system of claim 8, wherein the processor is a single-instruction multiple-data (SIMD) processor.

14. The turbo decoding system of claim 10, wherein the processor is a single-instruction multiple-data (SIMD) processor.

15. The turbo decoding system of claim 13, wherein the SIMD processor includes five processing elements for parallel processing, and wherein one of five processing elements controls the other four processing elements, processes scalar operation, and fetches, decodes, and executes instructions including control and multi-cycle scalar instructions, and wherein the other four processing elements only executes SIMD instructions.

16. The turbo decoding system of claim 14, wherein the SIMD processor includes five processing elements, and wherein one of five processing elements controls the other four processing elements, processes scalar operation, and fetches, decodes, and executes instructions including control and multi-cycle scalar instructions, and wherein the other four processing elements only executes SIMD instructions.

17. The turbo decoding system of claim 9, wherein the generated interleaved address is reused as a write address for writing the log likelihood ratio outputted from the SISO decoder into the LLR memory.

18. An interleaving method for rearranging data block in a data communication system, comprising:

preparing seed variables; and

generating interleaved addresses column by column using the seed variables.

19. The interleaving method of claim 18, wherein the seed variables are prepared when an interleaver structure changes due to the change of the coding

standard or bit rate, and generates the interleaved addresses column by column using the seed variables when the interleaved addresses are required.

20. The interleaving method of claim 19, wherein the seed variables include a base column vector, an increment column vector, a cumulative column vector, and a modulo base, the number of elements of all three column vectors is equal to the number of rows of the interleaver, and the elements of the column vectors are inter-row permutated, and

wherein the cumulative column vector is updated by adding the increment vector to the old cumulative vector, after the interleaved addresses for one column are generated by adding the base vector and a vector that is calculated from the cumulative vector, and

wherein if elements of the updated cumulative column vector are larger than the modulo base, the elements of the updated cumulative column vector is subtracted by the modulo base.